Amendments to the Claims

This listing of claims replaces all prior versions, and listings, of claims in the present application.

Listing of Claims:

Claims 1-20 (canceled)

21. (original) An arithmetic pipeline comprising:

a two input adder module, said module being controllable to add a first single precision floating point number to a second single precision floating point number and to output a resulting single precision floating point number, said module comprising:

means for inputting mantissa portions of the first and second single precision floating point numbers, said mantissa inputting means determining a larger number and a smaller number, and outputting a mantissa portion of the larger number and a mantissa portion of the smaller number;

means for inputting exponent portions of the first and second floating point numbers, said exponent portions inputting means determining and outputting a larger exponent;

means for inputting sign-bits of the first and second floating point numbers, said sign-bits inputting means determining and outputting a sign-bit for said resulting floating point number;

carry-in generation means for outputting carry-in data based on sign-bits of the first and second floating point numbers and the mantissa portion of the larger number;

addition logic receiving the carry-in data, mantissa of the larger number, mantissa of the smaller number, and a difference between the larger and smaller exponents, said addition logic shifting the mantissa of the smaller number to align with the mantissa of the larger number, calculating and outputting a normalized mantissa output and exponent modifier; and

output logic receiving the sign-bit result, the normalized mantissa output and the exponent modifier, said output logic outputting the resulting single precision floating point number based on the normalized mantissa output and exponent modifier.

22. (original) The arithmetic pipeline of claim 21, wherein all arithmetic negations are approximated to a logical negation and said carry-in generation means generates the carry-in data to correct the approximations.

23. (original) The arithmetic pipeline of claim 21, wherein said carry-in generation means generates the carry-in data to correct any loss of precision that may have occurred in shifting of the mantissa of the smaller number.

24. (original) The arithmetic pipeline of claim 21, wherein said carry-in generation means generates the carry-in data to correct incorrect determinations of which floating point number is larger.

25. (original) The arithmetic pipeline of claim 21, wherein said carry-in generation means generates the carry-in data to correctly round the resulting single precision floating point number to meet IEEE 754 rounding mode rules.

26. (original) An arithmetic pipeline comprising:

a flat four-input single precision floating point adder module, said module being controllable to add first, second, third and fourth single precision floating point numbers and to output a resulting single precision floating point number, said module comprising:

means for predicting a largest number from exponent and mantissa portions of said floating point numbers, said predicting means outputting a plurality of shifting data calculated based on said largest number and said exponent portions;

means for partially sorting said floating point numbers based on sign-bit and the exponent portions of said floating point numbers, said sorting means outputting sorted mantissas, sorted exponents, and sorted sign-bits;

carry-in generation means for outputting carry-in data based on said sorted sign-bits and mantissas;

addition logic receiving the carry-in data and said sorted mantissas and said plurality of shifting data, said addition logic calculating and outputting a normalized mantissa output and exponent modifier; and

output logic receiving the normalized mantissa output, exponent modifier, and a largest exponent, said output logic outputting the resulting floating point number based on the normalized mantissa output, the exponent modifier, and the largest exponent.

27. (original) The arithmetic pipeline of claim 26, wherein all arithmetic negations are approximated to a logical negation and said carry-in generation means generates the carry-in data to correct said approximations.

28. (original) The arithmetic pipeline of claim 26, wherein said carry-in generation means generates the carry-in data to correct any loss of precision that may have occurred in shifting of non-largest mantissas by said addition logic.

29. (original) The arithmetic pipeline of claim 26, wherein said carry-in generation means generates the carry-in data to correct incorrect determinations of which floating point number is larger.

30. (original) The arithmetic pipeline of claim 26, wherein said carry-in generation means generates the carry-in data to correctly round the resulting single precision floating point number to meet rounding mode requirements.

31. (original) The arithmetic pipeline of claim 26 further comprising a floating point multiplier module, said multiplier module inputs the input data and performs a multiply operation and said four-input single precision floating point adder module performs a normalization operation on a result of the multiply operation.

Claims 32-34 (canceled)